

LibreSilicon PT

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- A free and open source manufacturing process standard for semiconductors
- All the specs are public and don't require an NDA
- Supposed to be usable in a garage as well as in industrial environment
- Reproducible results due to open specification
- Also includes open source tools
 - Standard cell lib generation
 - Synthesis
 - Place and route
 - Simulation

- Mixed signal
- BJT and MOS transistors
- Diodes
- Diverse types of capacitors
- SONOS flash

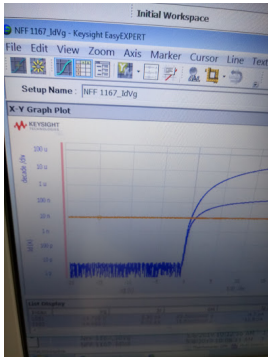
Factors hindering innovation:

- NDAs
- Vendor lock-in
- High costs for low-volume prototypes (up to 2000 Euros/mm² for 180nm nodes)

Security concerns

- Potential hard ware back doors
- Proprietary chips can't be audited by the public
- JTAG and other "features", compromising security

- Started process flow design in 2017
- Made the first test wafer (Pearl River) in 2018
- Fixed bugs with the process flow (2018-2020)

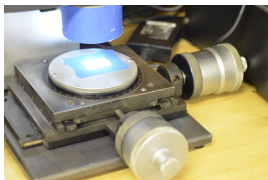


- Hong Kong protests
- The pandemic
- We ran out of funding (Renting the clean room)
- Other issues, forcing us to move to Portugal
- Issues with access restrictions to INL due to pandemic
- INL not setup to do CMOS manufacturing

- Building closed loop glove boxes
- Building a small maskless lithography unit using a DMD chip and a 445nm UV power LED
- Organizing funding for bench top mini CVD/RTP furnaces
- Setting up a process for 2 inch wafers in my garage
- Automatize the manufacturing (Robots for loading, unloading)
- Improve feature size, tackle immersion lithography

Maskless lithography

- Essentially a reverse microscope
- Lots of basic work done by Sam Zeloof
- Goal
 - Automatized stepping
 - Develop a product
 - Ship it to hobbyists



Glovebox setup

- Achievable with low material costs
- Clean room environment for limited spaces
- Can be used in a garage



- Explore new technologies
- Explore new applications
- Adapt garage setup to a foundry setup
- Offer a semiconductor prototype manufacturing service